

Faculdade de Engenharia da Universidade do Porto



Self-Calibrated Current Reference

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PREPARATION FOR DISSERTATION

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Abstract

The following document will be an introduction to the thesis “Self-Calibrated Current Reference”, and will help to prepare the work to be done in the future.

Current references are one of the key stones in most electronic circuits, but very few provide enough accuracy to be used in most modern and delicate systems. This document will explore the work done to solve these problems over the years. From the earliest appearances of the bandgap references into nowadays all CMOS architectures.

The state of the art in this document will be supplemented with a background and preliminary results chapter to better further the understanding of the problems faced.

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List of Abbreviations

List of abbreviations by alphabetical order

BJT	<i>Bipolar Junction Transistor</i>
BGR	<i>Band Gap Reference</i>
CMOS	<i>Complementary Metal–Oxide–Semiconductor</i>
CTAT	<i>Complementary To Absolute Temperature</i>
eV	<i>Electron-Volt</i>
MOS	<i>Metal-Oxide-Semiconductor</i>
MOSFET	<i>Metal–Oxide–Semiconductor Field-Effect Transistor</i>
PVT	<i>Process, Voltage and Temperature</i>
PTAP	<i>Proportional To Absolute Temperature</i>
ZTC	<i>Zero Temperature Coefficient</i>

Chapter 1

The following document will be split into five chapters. We will begin with a general introduction, followed by a more detailed background before we head into the main focus of this work.

Structure

This document will be divided in five sections:

- Introduction – In here it will be exposed how our work may be relevant to the developments of future current references, the motivation behind this work and the problems faced.
- Background – In this chapter we will expose the theory behind our work. This section we provide the background necessary to understand further chapters.
- State of Art – In here we will discuss the available solutions to this problem and how some solutions might be better than others. We will begin with the first topology of current references and finalize with the latest all CMOS topologies.
- Preliminary Results – This chapter will be dedicated to the simulation results of a few schematics. These simulations were conducted during the research to further understand the different topologies and compensation techniques.
- Work Schedule – Description of the work schedule and overview of the more important milestones.

Introduction

The increasingly high density of digital CMOS processes coupled with new advances in Digital Signal Processing is sparking a desire to implement mixed signal systems on a single chip. To realize a single chip implementation an accurate current reference is required to perform conversions between the analog and digital domains.

The current reference circuit is a key-stone in most electric equipment. Its sole purpose is to deliver an electric current. Now, this is easily done with a few MOSFETs, but the main goal of this work is to develop one that has an accuracy high enough to be used in more precise systems.

Some systems like operational amplifiers, data converters and phase-locked loops rely on current reference circuits to provide an accurate and stable current supply. Analog to Digital converters need a fixed reference for a measuring point for their sampling. Furthermore, high performance analog circuits require a stable bias point across a wide range of PVT conditions.

There has been a great deal of effort directed towards reducing the effects of temperature on the output of these devices. References are now being constructed that have very flat temperature responses and very little dependence on the power supply voltage. These references can easily have temperature dependences lower than 0.81% [1] over a 100°C range. In many cases it is the accuracy of the actual output voltages of identical devices that limits the performance of the system.

In regards to voltage compensation, it was known for a while and it still is one of the most used methods. We call it a self-biasing circuit that provides a supply independent voltage.

As we go deeper into higher integration technologies, a wider range of problems surface that need to be dealt with. The main focus of this thesis will be on the development of a current reference that has a 5% absolute precision over PVT conditions. A single MOSFET or a BJT possess a wide range of parameters that vary with PVT, thus affecting its performance, stability and long term reliability.

Chapter 2

Background

In this chapter, we will be exposing the knowledge necessary to understand the following sections. We will be analyzing different voltage and current references topologies, resistor architectures, along with several compensation techniques to both temperature and voltage.

2.1 Voltage Reference Architectures

Voltage references are one of the most used blocks in many PVT insensitive current references. There are a number of characteristics that are desirable in a high quality voltage reference. It is important that the reference can deliver a very constant voltage over many varying conditions. Changes in the supply voltage should not cause significant changes in the output voltage of the reference. The effects of temperature on the output of the device should also be minimal. Finally, two identical references should have the same output characteristics, under the same technology.

There are various different methods of designing a voltage reference. Of these there are about three major categories that the different designs can fall into. These categories generally describe either the technology in which the reference is constructed or the method of deriving the constant output voltage.

In MOS technologies the most obvious way of deriving a reference is through the use of the threshold voltage. Very accurate references often use buried Zener diodes. In strictly bipolar processes, the emitter base junction of a BJT can be used to derive the bandgap voltage of silicon for use as a reference voltage. Finally, it is possible to create bipolar transistors, in a MOS process, that are adequate to extract the bandgap voltage of silicon. These can be used with other MOS circuitry to produce a reference voltage.

2.1.1 MOS Only References

Since there has been a big push to implement mixed signal applications in a single CMOS chip there have been numerous different attempts to design good voltages references using only CMOS components. The most obvious technique of producing a CMOS reference is to use two different threshold voltages to find a constant voltage. [2] [3]

The threshold voltage V_{th} can be generically modeled by the following expression

$$V_{th} = V_{t0} + \alpha T \quad (1)$$

Where, V_{t0} is the basic threshold voltage at absolute zero and α is the temperature factor of the MOS device. If a process exists in which there are two different threshold voltages for the same type of device, then these two values can be subtracted to produce a constant reference value. If the devices are of the same type it is assumed that they will have similar temperature responses but different V_{t0} .

The gate voltage V_{GS} of a MOSFET device is given by

$$V_{gs} = \sqrt{\frac{I_{ds}}{K}} + V_{th} \quad (2)$$

If I_{ds} and K are the same for the two different types of transistor then the difference between their gate voltages will give an output that is strictly the difference between their threshold voltages. A circuit that extracts this difference can be seen in figure 2.1.1.

In the following figure the transistor that is circled is the device that has the lower threshold voltage. The feedback in the circuit will strive to make the two inputs of the op amp equal. If the two resistors are matched they will have identical currents when the op amp inputs become equal. This implies that the currents through the MOSFETs will be equal. The op amp must set V_{gs2} to achieve this equal current condition. The output voltage will be the difference between V_{gs1} and V_{gs2} which is strictly the difference between their threshold voltages.

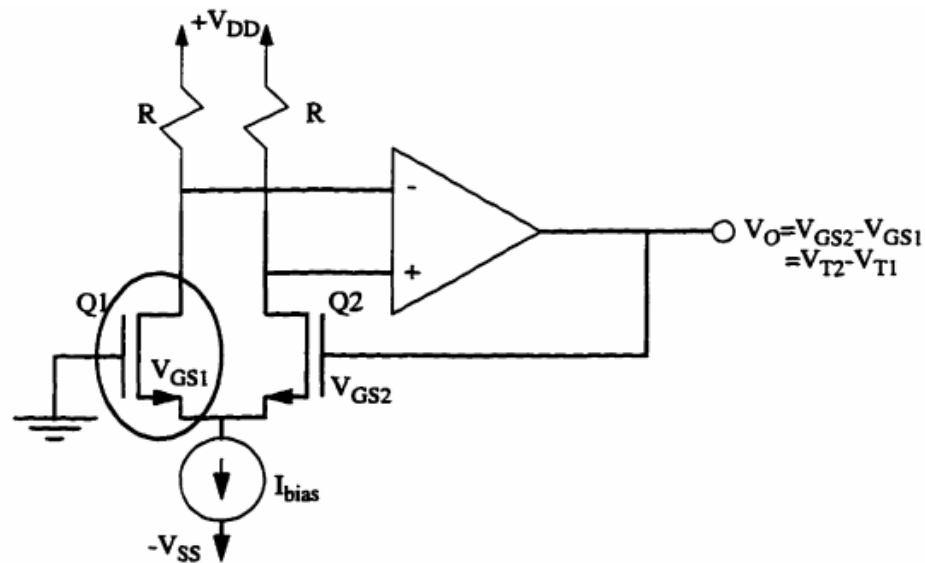


Figure 2.1.1 - MOS Voltage Reference

2.1.2 Buried Zener References

The most basic type of reference that can be constructed uses the reverse breakdown voltage of a zener diode. An example of a simple zener reference circuit is shown in figure 2.1.2. This type of reference can usually be made very accurately. The reference has very little dependence on the supply but it does have a fairly strong temperature dependence. Another major problem with this reference type is the large amount of noise generated by a diode in its Zener breakdown region. Some of this noise can be eliminated if the zener diode is buried in the substrate away from the surface giving rise to buried Zener references. [4]

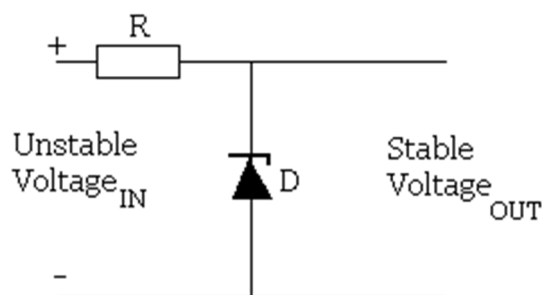


Figure 2.1.2 – Zener Voltage Reference

2.1.3 Bandgap References

A bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. It produces a fixed voltage irrespective of power supply variations, temperature changes and the loading on the device. Depending on the technology, it has an output voltage around 1.25 V, close to the theoretical 1.22 eV bandgap of silicon at 0 K.

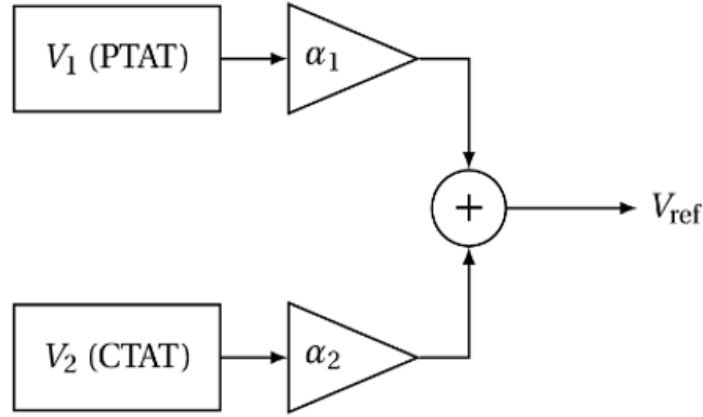


Figure 2.1.3.1 – Temperature Compensated Voltage Reference Model

The idea behind this type of circuit is generically modeled in figure 2.1.3.1. The idea is that with V_1 and V_2 having a very well defined dependency with temperature, we can add both voltages in order to “eliminate” the temperature dependency factor. From the equations 3 and 4 we can see that adding these two voltages would give a voltage reference and its overall variation over temperature would be ideally zero.

$$V_{ref} = \alpha_1 V_1 + \alpha_2 V_2 \quad (3)$$

$$\alpha_1 \frac{dV_1}{dT} + \alpha_2 \frac{dV_2}{dT} = 0 \quad (4)$$

This type of references use the base emitter junction of two or more bipolar transistors to extract the 0K bandgap voltage. The voltage across the base emitter junction of a transistor, for a collector current I_{co} and a temperature T_o is given by,

$$V_{be} = V_{go} \left(1 - \frac{T}{T_o} \right) + V_{be0} \left(\frac{T}{T_o} \right) - \frac{nkT}{q} \ln \left(\frac{T}{T_o} \right) + \frac{kT}{q} \ln \left(\frac{I_c}{I_{co}} \right) \quad (5)$$

Where V_{go} is the bandgap voltage of the silicon at 0K which is typically 1.17V but subjected to the technology in use, and V_{be0} is the base emitter voltage of the transistor at I_{co} and T_o . The third term containing the natural logarithm of T is small and can be ignored in first order approximations. The following figure shows the V_{be} variation with collector current over a wide range of temperature.

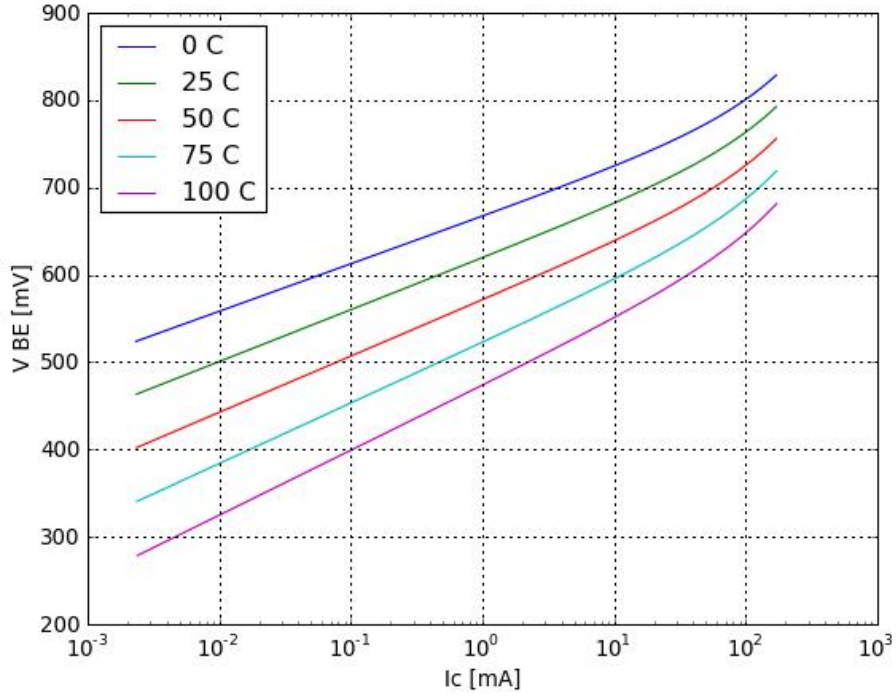


Figure 2.1.3.2 – Base-Emitter Voltage Variation for multiple Temperatures

From equation 5 and after analyzing figure 2.1.3.2 we can clearly see that V_{be} lowers as temperature goes up. We say that this voltage is **complementary to absolute temperature** (CTAT). Its slope is technology dependent but its value is usually around -1.7 mV/K .

Differential V_{be}

A circuit capable of creating a voltage proportional to absolute temperature can be used to cancel the temperature dependence of the base-emitter voltage. This will create a reference voltage that is essentially independent of temperature variations.

For two transistors biased with different collector currents (I_C) all the terms in equation 5 are the same except for the last term $\frac{kT}{q} \ln\left(\frac{I_C}{I_{C0}}\right)$. Therefore, if we take the difference between two base emitter voltages we get,

$$V_{be1} - V_{be2} = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C0}}\right) - \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C0}}\right) \quad (6)$$

$$\Delta V_{be} = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}}\right) \Leftrightarrow \Delta V_{be} = \frac{kT}{q} \ln(N) \quad (7)$$

And while V_{be} is CTAT, from equation 7 we clearly see that the difference between two V_{be} is **proportional to absolute temperature** (PTAT). From equation 8 we can see that the PTAT voltage is around 0.09 mV in the first order approximation.

$$V_t = \frac{\Delta V_{be}}{\ln(n)} \Leftrightarrow \frac{\partial V_t}{\partial T} = \frac{\partial \left(\frac{kT}{q}\right)}{\partial T} = \frac{k}{q} \approx 0.09 \text{ mV} \quad (8)$$

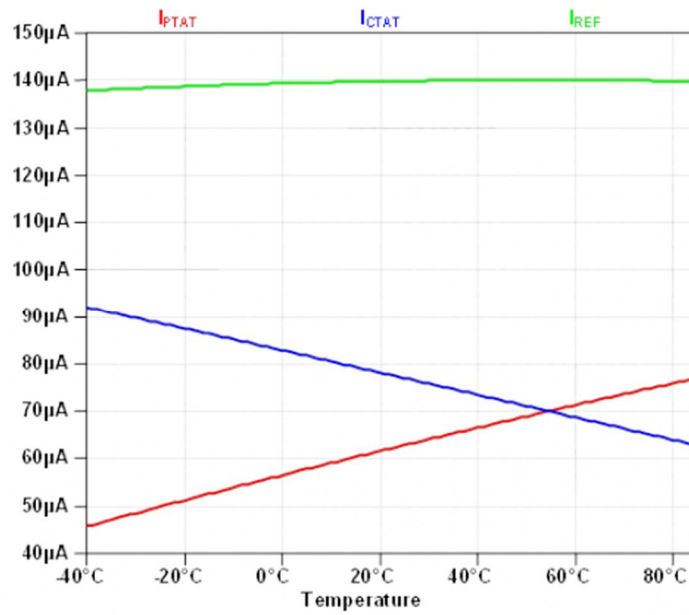


Figure 2.1.3.3 – PTAT + CTAT

Thus, we can add the Vbe voltage (CTAT) and the difference between two Vbe (PTAT) to achieve the temperature independent voltage. This can be seen in figure 2.1.3.3 in which a CTAT (blue) is added to a properly weighted PTAT (red) voltage.

2.1.4 Zero Temperature Coefficient Point

The Zero Temperature Coefficient Point or simply ZTC point is what we call a certain voltage level that when applied to the gate of a MOS device will nullify temperature dependence. The threshold voltage and the carrier mobility of a mosfet are dependent on temperature. [14]

For carefully sized nMOS transistors with channel doping concentration on the vicinity of 10^{15} the output current (I_{ds}) becomes temperature independent.

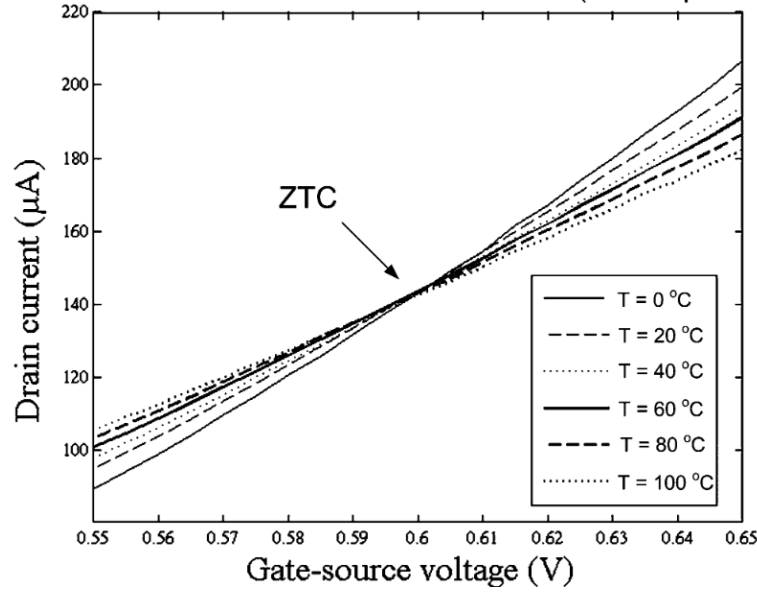


Figure 2.1.4.1 – V_{gs} vs. I_{ds} for an array of Temperatures

As we can see in the figure above, by biasing the gate voltage of a mosfet at approximately 0.605 V, the device will provide a current that is invariant to temperature shifts. This type of compensation works similarly to the PTAT and CTAT sum since with precise sized mosfets, the internal temperature dependences cancel each other out.

The mosfet current is modeled by,

$$I_d = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_{gs} - V_{th})^2 \quad (9)$$

In equation 9, the carrier mobility (μ) and the threshold voltage (V_{th}) are the major temperature dependent parameters. Both of these quantities diminish as the temperature goes up. However, they have an opposite effect on the drain current. As the mobility goes down, so does the current. But, as the threshold voltage goes down, the drain current goes up due to the ($V_{gs} - V_{th}$) difference.

The ZTC bias point is a certain voltage level in which the changes in electron mobility and threshold voltage compensate each other. A transistor biased at this point will have minimal variation in its saturation current over temperature.

2.2 Resistor Architectures

Either we wish or not, this type of circuits will always need some type of resistor to produce the desired current. There are three solutions for this problem.

The first solution is using a MOSFET in ohmic mode, thus the name of this region. A MOSFET can operate as variable resistor although there are several drawbacks. The linearity is poor and is dependent of the input voltage.

The second solution is simply using a physical resistor and the problem is solved. There are a few disadvantages with using a resistor in high level integrations. Take for example a supply voltage of 1.25 V, like the standard bandgap reference, and you wish an output current of 100nA. This would require a 12.5M Ω which would take a lot of area in the die. Not to mention the resistors are non-linear and the tolerances are large.

This is mostly due to the fact that there isn't a standard CMOS fabrication procedure for resistors. Instead, we use the layers in the integrated circuit. These layers can range from simple aluminum to polysilicon. Each material has its own properties that will influence the resistor value and its variations.

In CMOS technology, a resistor is defined by a constant called sheet resistance. For the standard 0.18 μm CMOS technology this has a value of 290 $\Omega/\mu\text{m}^2$ for the N+ polysilicon.

If we take into account the previous resistor of 12.5M Ω we would need an area of approximately 1 μm x 43000 μm .

Not to mention that in the same circumstances this material has a temperature constant -1350 ppm/ $^{\circ}\text{C}$ in the first order approximation.

A resistor using sheet resistance in regards to temperature variation can be calculated by,

$$R(T) = R_{\text{sheet}}(1 + T_{\text{cr}1}(T - T_0) + T_{\text{cr}2}(T - T_0)^2 + \dots + T_{\text{cr}n}(T - T_0)^n) \quad (9)$$

Where, $T_{\text{cr}n}$ are the constants corresponding to each level of approximation and T_0 is a constant temperature in which the difference is measured. Just using the second order approximation using the same sheet resistance we come up a 6.2% deviation of the resistor value due to a 75 $^{\circ}\text{C}$ shift.

Not to mention that there are large variations due to the geometry later on, requiring specific layout design techniques such as inter-digitization and cross-couple to try to lower these variations.

2.2.1 Switched-Capacitor Resistor

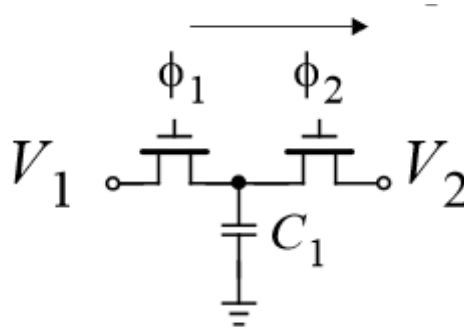


Figure 2.2.1.1 – Switched-Capacitor Resistor Circuit

The other option, and the most obvious solution to large resistors, is the use a switched-capacitor resistor, shown in figure 2.2.1.1. Instead of using a physical resistor, we can “simulate” one by controlling the charge and discharge of a capacitor. This circuit simulates the behavior of a normal resistor, with a few added benefits. [1][6][8]

The capacitor ratios can be tightly controlled, providing a more stable current overall, and by controlling the signal going into ϕ_1 and ϕ_2 , we can control the value of the resistor and thus, change the current output.

Although this is a viable solution to higher levels of integration, it also brings a few more parameters to take into account during the development, like clock feedthrough and charge injection cancellation, not to mention the necessity of an external signal to clock the capacitors.

$$Req = \frac{1}{c1f} \quad (7)$$

The equivalent resistor value of the figure 2.2.1.1 is given by the inverse of capacitance times the switching frequency. If we want a 12.5M Ω we would simply need a 10MHz clock and a capacitor with 0.08pF.

Both MOSFETs used in the previous schematic are used as switches to control the charge and discharge of the capacitor. MOSFETs are considered good switches because of two main reasons:

- Off-resistance near G Ω range (subjected to technology). At lower nodes leakage increases so it must be taken into account.
- On-resistance in 100 Ω to 5k Ω range, depending on transistor sizing.

These type of circuits requires non-overlapping signal to both switches, requiring another component to the system. Figure 2.2.1.2 shows such component. Both ϕ_1 and ϕ_2 need to be non-overlapping to properly control that charge and discharge of the capacitor.

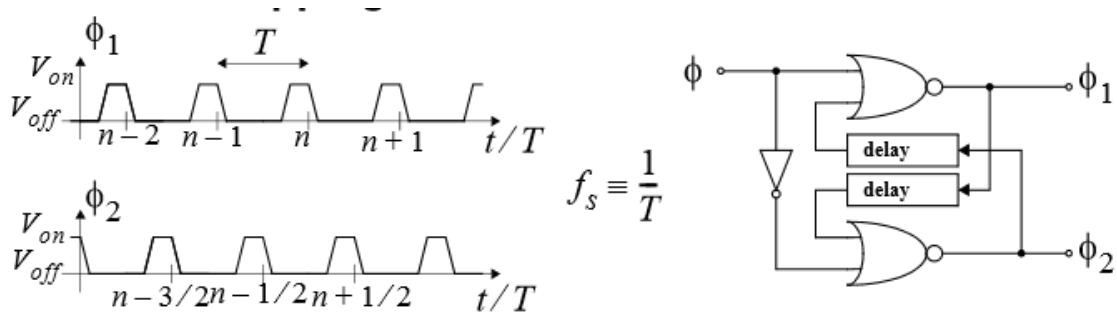


Figure 2.2.1.2 – Non-Overlapping Clock Generator

Clock Feedthrough

One of the main disadvantage of this resistor architecture are the parasitic capacitances between the gate-drain and gate-source. Depicted in figure 2.2.1.3, the effect introduces an error in the samples output voltage.

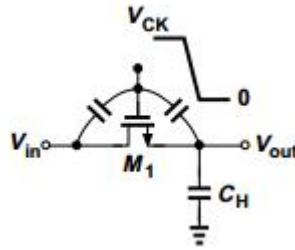


Figure 2.2.1.3 – Parasitic Capacitances of MOSFET

Assuming that the overlap capacitance is constant, we have an error of,

$$\Delta V = V_{ck} \frac{WCov}{WCov + Ch} \quad (8)$$

where Cov is the overlap capacitance per unit width. The error ΔV is independent of the input level, manifesting itself as a constant offset in the input/output characteristic

Channel Charge Injection

Another problem we face with this architecture is the charge injection when the MOSFET is “turned on”.

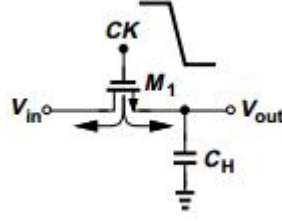


Figure 2.2.1.4 – Channel Charge Injection Representation

As depicted in figure 2.2.1.4, the charge injected to the left side is absorbed into the input source, creating no error. On the other hand, the charge injected to the right side will be deposited on C_H , introducing an error voltage stored on the capacitor. This error is modeled in equation 9.

$$\Delta V = \frac{WLCox(V_{dd} - V_{in} - V_{th})}{2C_H} \quad (9)$$

A practical way to solve this problem would be using low input voltages and larger capacitors. Another possible answer would be using complementary switches instead of a single MOS device to increase the resistance.

Thermal Noise

Since one of main goals of this work is to minimize PVT variations we also need to take into account the thermal noise. The on-resistance of MOSFET switch will introduce thermal noise at the output and, when switch turns off, this noise is stored on the capacitor. This voltage is given by equation 10 and can be controlled by employing larger capacitors.

$$Noise\ Voltage = \sqrt{\frac{kT}{C}} \quad (10)$$

Like the previous effects, larger capacitors would require smaller frequencies, so it would be a trade-off between speed and precision.

Chapter 3

State of the Art

In this section we will be presenting the state of the art solutions to the problems explained in the introduction. Some of the solutions here exposed will sometimes sacrifice a precision in one element in favor of another. A high precision circuit like this should always have in mind the system in which it will be integrated.

3.1 Traditional Bandgap Voltage Reference

We begin our research with the simplest and one of the oldest model of BGR (Bandgap Reference), depicted in the figure below. It's worth noting that while this design was released a long time ago it's still one of the most used today or, at least, the general idea behind it. [15]

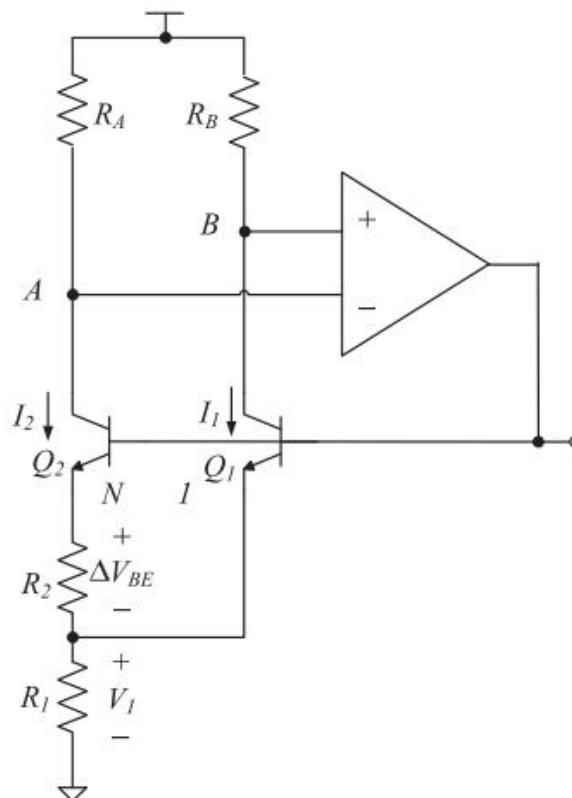


Figure 3.1 simplified Brokaw bandgap voltage reference circuit
(Brokaw, 1974)

This architecture uses the concept explained in section 2.1.3. To compensate the temperature it extracts the CTAT voltage from V_{be} of the bipolar transistor, and the PTAT from the ΔV_{be} of both BJTs. Thus, by adding these two voltages we arrived at a voltage level with very low dependency on temperature.

The operational amplifier forces the voltages levels at V_A and V_B to be equal. If both resistors R_A and R_B are matched then the same current flows on both branches of the schematic.

Since R_1 is the sum of two identical currents, we can write:

$$V_1 = 2 * IR_1 \Leftrightarrow V_1 = 2 * R_1 * \frac{\Delta V_{be1,2}}{R_2} \quad (11)$$

Since $V_{ref} = V_{be1} + V_1$, thus:

$$V_{ref} = V_{BE1} + \left(\frac{2 * R_1 \ln N}{R_2} \right) V_t$$

In which, N is the ratio between both bipolar transistors.

By adjusting the relation between R_2 and R_3 but also the areas of both BJT we can adjust the slope of the PTAT voltage to better eliminate temperature dependency. This design is also highly insensitive to supply changes due to the need of equal currents in both branches, this achieved by the amplifier.

3.2 MOS Biased Bandgap Voltage Reference

Another familiar model is presented in [16]. It replaced the bias resistors and amplifier with a self-biased current mirror as it is shown below. It works similar to that of figure 3.1 with the exception that the feedback loop was replaced by the transistors Mp1, Mp2, Mn1 and Mn2.

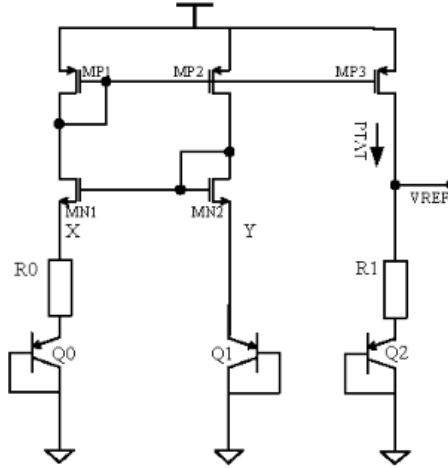


Figure 3.2 Self Biased BGR Architecture
(From [16] page 1)

Since MP1 and MP2 have the same VGS, by selecting SP1 = SP2, we shall obtain IDmp1 = IDmp2. As a result, the currents flowing through Mn1 and Mn2 should be the same. If we do not consider the short channel effect, the drain voltages of Mp1 and Mp2 will be the same. Since the gates of Mn1 and Mn2 are connected together, by selecting SMn1 = SMn2, we shall obtain IDMn1 = IDMn2. As a result, Ix = Iy which yields,

$$V_{eb1} = V_{eb0} + R_0 * I_x \quad (12)$$

$$I_x = \frac{V_{eb1} - V_{eb0}}{R_0} = \frac{\Delta V_{eb0,1}}{R_0} \quad (13)$$

Since, Ix = Iq0 and Iy = Iq1, and the emitter area ratio between both BJT transistors is N then,

$$I_x = I_y = \frac{V_t * \ln(N)}{R_0} \quad (14)$$

Finally, since IPTAT = Ix we can write,

$$V_{REF} = I_x * R_1 + V_{eb2} \quad (14)$$

As we go into higher integration, the self-biased mirror would suffer from channel modulation, thus highly increasing supply dependency.

3.3 Low-Voltage Voltage Reference

A slightly improvement over both the previous references is the one presented here. This improvement comes in the way of lowering the supply voltage necessary to produce the PVT voltage. Of course this also lowers the bandgap voltage itself to around half of the theoretical value. [11]

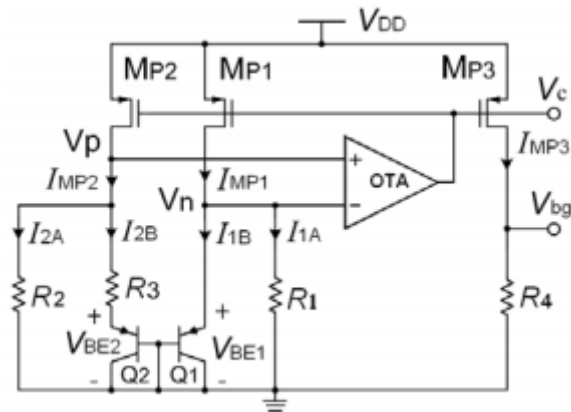


Figure 3.3 – Low-Voltage Voltage Reference
(From [11] page 3)

The output of this bandgap reference is 611.9 mV with a variation of 0.8mv. Using lower voltages in higher levels of integration will slightly lower the short channel effects of the MOS devices but also increase devices longevity by lowering their stress limit.

This improvement comes from folding the conventional BGR circuit to ground on nodes Vp and Vn. If resistors R1 and R2 are matched, then the same current will flow from both branches, $I_{2A} = I_{1A}$. The operational amplifier also clamps both Vp and Vn to equal voltage levels. Since,

$$V_p = V_n = V_{be1}, V_{r3} = V_{be1} - V_{be2}, I_{mp2} = I_{2A} + I_{2B} \quad (14)$$

$$Imp2 = \frac{V_{be1}}{R2} + \frac{\Delta V_{be}}{R3} = \frac{V_{be1}}{R2} + \frac{V_t \ln(N)}{R3} \quad (15)$$

Thus we can write,

$$Vbg = m \left(\frac{Vbe1}{R1} + \frac{Vt * \ln(N)}{R3} \right) R4$$

Where m is number of times the ratio of MP3. By properly adjusting the values of the resistors and BJT areas we can achieve 611.9 mV with an accuracy of 0.13%.

3.4 Current Reference Architecture

A current architecture to generate a current source is shown below. This architecture refers only to the conversion between a voltage level and its current supply. This topology requires a bandgap reference and works by controlling a certain dump of energy in node 1. [17].

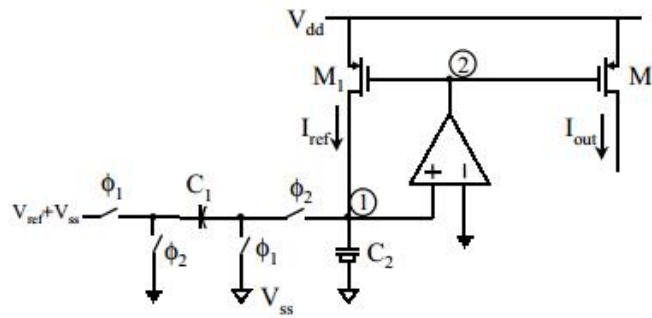


Figure 3.4 – Current Reference Architecture
(From [17] page 1)

During ϕ_1 , C_1 charges to V_{ref} . During ϕ_2 this charge is dumped on node 1. Thus, the ripple voltage is

$$\Delta V = -\left(\frac{2C_1}{C_1 + 2C_2}\right)V_{ref}$$

The ripple voltage can be lowered by increasing the value of C_2 . A large C_2 reduces at ripple at the expense of increased die area. The current delivered by the switched-capacitor is approximately

$$I_{ref} = C_1 * V_{ref} * F_{clk}$$

This architecture offers an accuracy of 0.029%. Further improvement to this topology can be made by placing an amplifier connected in M_2 to increase the output resistance. Another improvement will be the addition of a filter between the amplifier output, node 2, and the gate of M_2 .

3.5 Switched-Capacitor Current Reference

A realization of a current source using the bandgap reference presented in section 3.3 and a modification of 3.4 is shown below. One of the latest available types of current references with low variation over PVT parameters uses the above described components. According to [1], a low dependence PVT circuit is presented. It was projected using 0.13um CMOS technology and provides an overall precision of $\pm 3\%$ over PVT conditions.

One factor that we must take into account when using switched-capacitors is the frequency response of the system. This model has an 8us settling time, meaning that once this circuit was powered, its output is only reliable after the settling time has been achieved.

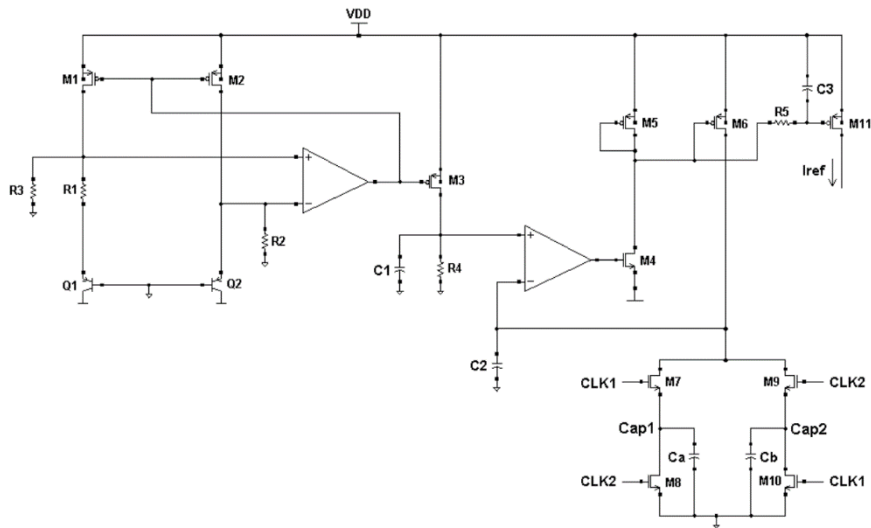


Figure 3.4 – Switched-Capacitor Current Reference Schematic
(From [1] page 2)

This architecture is depicted in figure 3.4 and we can easily identify the three general blocks that compose this system. At the top left we have the traditional bandgap voltage reference to provide PVT invariant voltage, this version is the low voltage in section 3.3.

This reference voltage is fed into a voltage to current converter on the top right. The final piece of this schematic is the switched-capacitor resistor on the bottom right. This resistor is controlled by the CLK1 and CLK2 signals to adjust the resistor value and output current.

This current reference uses the PTAT and CTAT currents from the bipolar transistors, generating a voltage insensitive to both temperature and supply voltage.

It's worth noting that the current source here applied uses a filter between M6 and M11 to reduce the ripple voltage.

$$I_{ref} = 2 * V_{bg} * C_a * F_{ref}$$

The output current is given by the previous equation in which, V_{bg} is the bandgap voltage, C_a is the value of the capacitor and F_{ref} is the working frequency. The factor 2 comes from the simulated parallel resistors of C_a and C_b . If both capacitors have the same value, then the resistance is cut in half.

This topology has a 3% variation over PVT. This error is mainly dependent of the offset voltage from the operational amplifiers and the ripple voltage.

3.6 All MOSFET, Two Resistor Current Reference

There have been many proposed current references through the years, and as we go into higher integrations, the resistors don't scale as well as MOSFETs. The next step in current reference construction was the idea of trying to eliminate virtually all resistors, resorting only to transistors.

To minimize production costs, this architecture uses no BJTs, external components or trimming procedures. This circuit was designed for 22nm technology and simulations results show a PVT tolerance of around 10%. The main advantages of this circuit is the low voltage operation, suitable for sub-micron applications due to reduced electrical stress limit. [9]

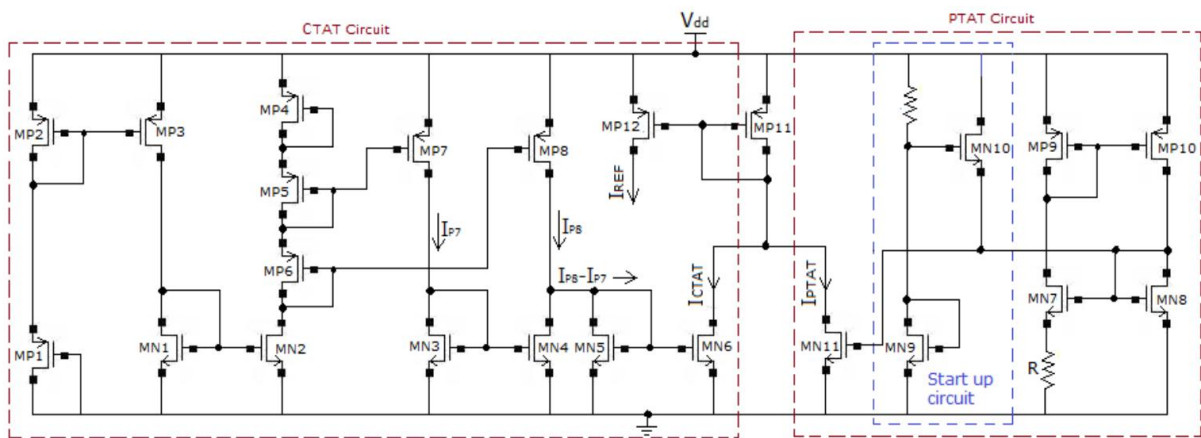


Figure 3.6 – All MOSFET, Two Resistor Current Reference Schematic
(From [9] page 3)

The architecture is shown in figure 3.6. In the schematic, we can see some of the basic modules like the PTAT circuit whose current is generated by a Beta multiplier reference with the exception of MN7 and MN8 being in weak-inversion and the startup circuit necessary for setting the operating point.

Since transistors MN7 and MN8 are working in weak-inversion, their current is governed by a different equation from before. In weak-inversion the current is given by,

$$I_{n8} = I_0 \frac{W_{n8}}{L_{n8}} e^{\frac{V_{gs8} - V_{th}}{nV_t}}$$

Using $N_8 = A_{N7}$, and $V_{gs8} = V_r + V_{gs7}$ we can write the current in MN8 as,

$$I_{n8} = I_0 \frac{W_{n7}}{L_{n7}} e^{\frac{V_{gs7} - V_{th}}{nV_t}} * e^{\frac{V_r}{nV_t}} \Leftrightarrow I_{n8} = I_{n7} * A * e^{\frac{V_r}{nV_t}}$$

$$V_r = nV_t * \ln\left(\frac{S_{n7}}{S_{n8}} * \frac{S_{p10}}{S_{p9}}\right)$$

Solving for V_r , we arrive at voltage value that is clearly PTAT and very similar to the differential base emitter voltage of two BJT. The slope of the voltage can be adjusted using the size ratios of the four transistors.

The CTAT current generated to eliminate the temperature dependency is the difference of two others. To eliminate the process dependency, the MOSFET seven and eight were properly scaled to arrive at a theoretical 0% process dependency.

This topology is viable to high integrations as this architecture is technology independent and allows integration into 22nm and beyond. However, it suffers from low accuracy by working in sub-threshold region of operation. In this region temperature dependence suffers from high non-linearity and thus reports only an accuracy of 10% over PVT.

A suggestion to be analyzed further in order to improve this circuit would be replacing the resistor R by a switched-capacitor resistor, lowering its variation and providing a more accurate PTAT current.

3.7 Resistorless Current Reference

The last step in current reference architecture would be a Resistorless current reference. A resistorless circuit allows for higher integrations all the while simplifying the circuit layout and area consumption. A resistorless current reference source is depicted in figure 3.7. [10]

This circuit uses cascode structures to improve the power supply rejection ratio. The reference current source has been designed in 65 nm technology. The presented circuit achieves 55 ppm/°C temperature coefficient over range of -40 °C to 125 °C. Reference current susceptibility to process parameters variation is $\pm 3\%$. The power supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz is lower than -127 dB and -103 dB, respectively.

The current reference source presented here consists of MOSFETs and vertical p-n-p bipolar transistors. It is designed for 3.3 V supply voltage with low sensitivity to process variation and small temperature coefficient.

Temperature independency is achieved by obtaining appropriate temperature coefficients of the summed currents I_1 , the PTAT current and I_2 , the CTAT current.

Low sensitivity to supply voltage bases on using cascode structures. Transistors MB1-MB13 form bias block which provide bias voltage to cascode structures and bulk node of M8. Moreover, transistors MB9-MB13 work as start-up circuit.

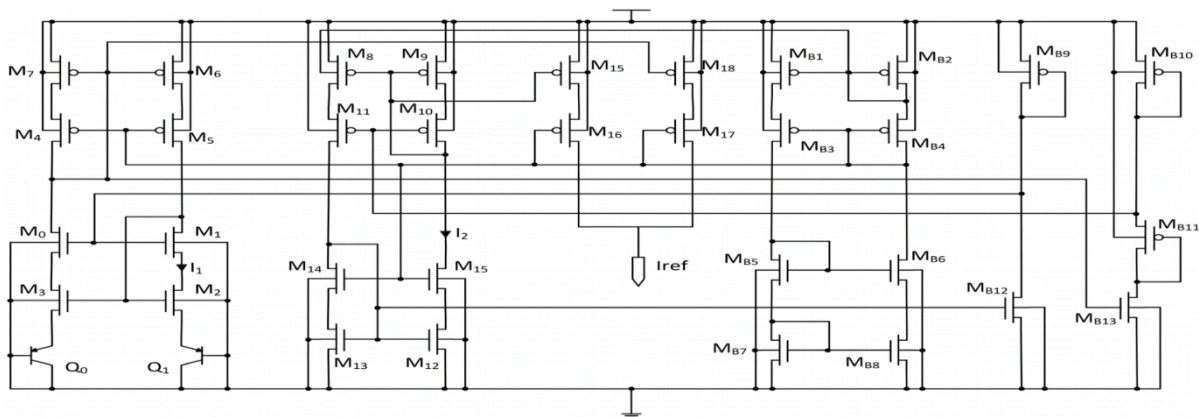


Figure 3.7 – Resistorless Current Reference Schematic
(From [10] page 2)

That PTAT current is achieved using the difference between the base emitter voltages of Q0 and Q1. This current can be easily adjusted by changing the sizes of both M3 and M2 but also the areas of both BJT. This current is given by,

$$I_{ptat} = \frac{\mu C_{ox}}{2} * \frac{\left(\frac{kT}{q} \ln\left(\frac{A_0}{A_1}\right)\right)^2}{\left(\sqrt{\frac{L_3}{W_3}} - \sqrt{\frac{L_2}{W_2}}\right)^2}$$

The CTAT current is formed by transistor M8-M15 and is based on threshold voltage difference. The difference is obtained by using the body effect.

$$I_{d8,9} = \frac{\mu C_{ox}}{2} * \frac{W_{8,9}}{L_{8,9}} (V_{gs} - V_{th})^2$$

Since $V_{gs} = V_{gs8} = V_{gs9}$, and solving V_{gs9} and substituting in V_{gs8} we arrive at:

$$I_{ctat} = \frac{\mu C_{ox} W_8 W_9 (V_{th8} - V_{th9})^2}{2(\sqrt{L_8 W_9} - \sqrt{L_9 W_8})^2}$$

The summation of both currents is made in the transistors M15-M18. The variation in this architecture comes from the non-linearity of both currents.

3.8 4-Bits Trimmed CMOS Bandgap Reference

Every single architecture we have seen until relied primarily on analog design. The matching of transistors with proper weighing, the sum of CTAT and PTAT currents and cascodes structures. However, there is another type of architectures. In these topologies, we use a more digital approach by adding trimming procedures.

Although these trimming procedures usually increase the accuracy of the architecture, they also have several disadvantages like the increase in die consumption and the need of external digital signals to drive the latches.

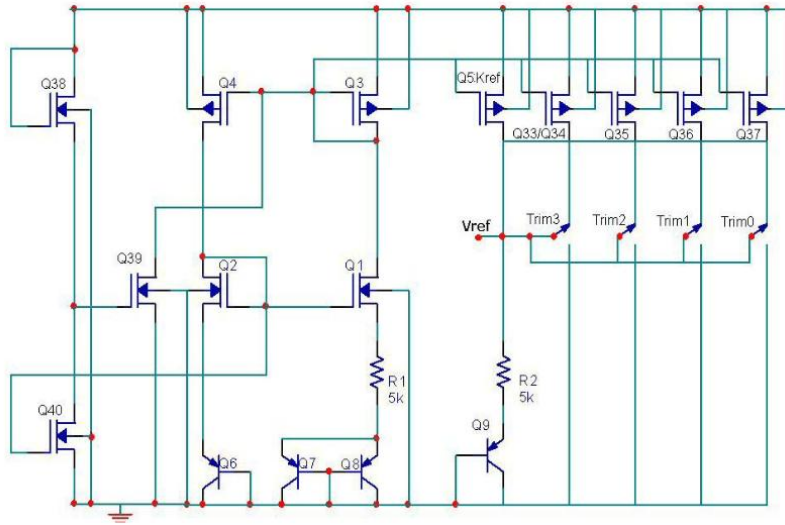


Figure 3.8 – 4-bit trimmed CMOS Voltage Reference
(From [18] page 3)

Before we head into the trimming procedures let us first observe the remaining circuit. The bandgap voltage core is identical to that of section 3.2. They extract CTAT from V_{be} and PTAT from the differential base emitter voltage of BJT. A small difference is Q7 and Q8 are split into two, parallel connected BJTs instead of a single transistor, to slightly lower process dependency.

Trimming is the concept of shutting down parts of the circuit in order to benefit the overall goal. In this design, we use the standard bandgap voltage reference with Q1-Q8. Q38-Q40 represent the startup circuit. The last four mosfets (Q34-Q37) can be disconnected from the circuit in order to improve process independence.

Let's us assume that we have an ideal output of 1.2V and the worst case of expected variation is 5%. The number of trimming bits necessary is given by,

$$n \text{ bits} = \frac{\ln\left(\frac{1.2}{0.05 * 1.2} + 1\right)}{\ln 2} \geq 3.41 = 4 \text{ bits}$$

Transistors Q34-Q37 are parallel connected to Q5, the mosfet responsible by driving ΔV_{be} into R2. By switching Q34-Q37 to on or off states we can adjust the current flow through R2. Since there are 4 available bits, this gives us 16 levels.

3.9 Overview

From the relevant architectures and compensation techniques we have seen, I would like to point out that every circuit regarding insensitive temperature relies always on the same technique, that one being the sum of two, opposed scaling, temperature dependent currents to remove the variance.

Another technique is called the ZTC point. Instead of summing two currents, we try to bias the MOS device at a specific voltage in which its internal parameters automatically cancel each other out, temperature wise of course. Although, sometimes such bias point is difficult or even impossible to find.

Supply independence can be achieved mostly by two ways. The first is using the traditional bandgap reference. The voltage reference is achieved by extracting the bandgap silicon voltage, this value being independent of the supply itself seeing it's a physical constant of the silicon itself. The other solution is the use of cascode structures to increase the PSRR (Power Supply Rejection Rate), like the Wilson current mirror that offers very small supply dependence.

Process compensation it's difficult to do. The techniques are usually based on optimal transistor matching and intelligent layout design. Prioritizing circuit symmetry is usually the best way to go.

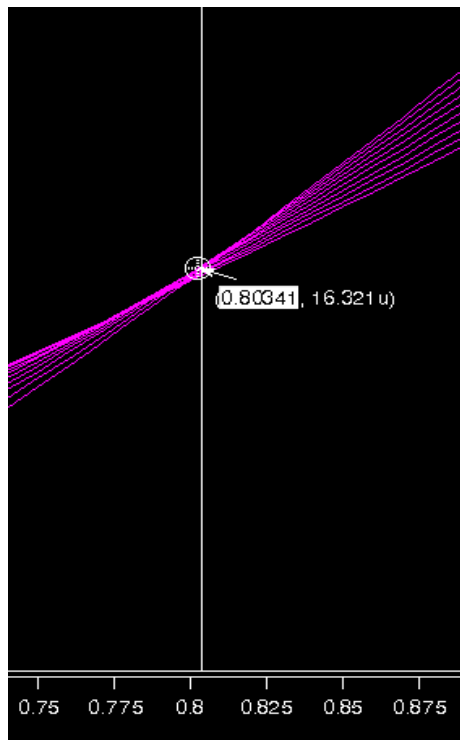
Ref.	Technology	Techniques Used	Devices	Compensation	Output	Area mm^2	Accuracy (%)
[1]	0.13 μm	PTAT+CTAT Switched-Capacitor	MOSFET BJT	PVT	16.07 μA	-	0.6
[12]	0.18 μm	Switched-Capacitor	MOSFET	PVT	6.88 μA	-	0.029
[11]	0.35 μm	PTAT+CTAT	MOSFET BJT	PVT	612 mV	0.117	0.327
[9]	22 nm	PTAT+CTAT	MOSFET	PVT	82 μA	-	5
[10]	65 nm	PTAT+CTAT Cascode Structures	MOSFET BJT	PVT	6.46 μA	-	3
[2]	0.5 μm	PTAT+CTAT	MOSFET	VT	2.670 V	0.01	1
[3]	0.25 μm	Cascode Structures PTAT+CTAT	MOSFET	VT	10.45 μA	0.002	1
[13]	0.18 μm	PTAT+CTAT	MOSFET	PVT	58 μA	-	1,38
[14]	0.18 μm	ZTC	MOSFET BJT	PT	144.3 μA	-	7
[18]	0.35 μm	Trimming	BJT	PVT	1,23V	0.140	1%

Table 3.1 Comparison between Current/Voltage References

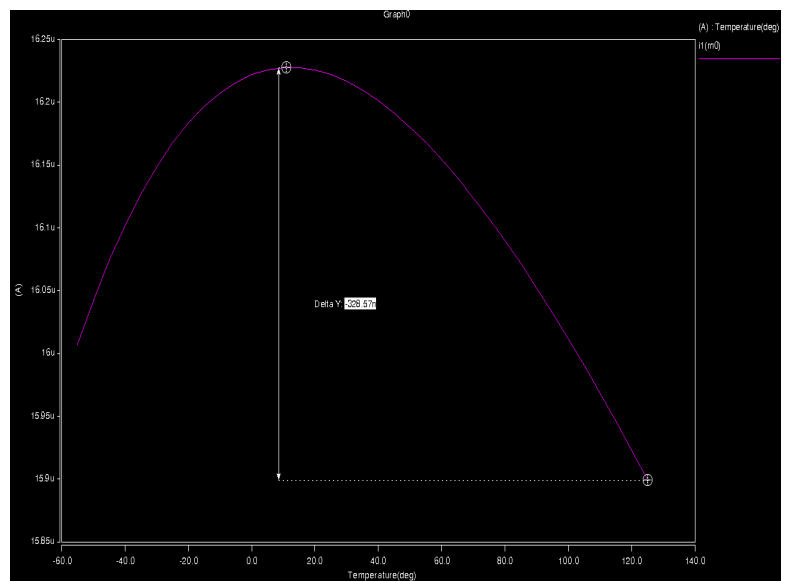
Chapter 4

Preliminary Results

ZTC Bias Point



(a)



(b)

Figure 4.1 V_{gs} vs. I_{ds} over several Temperatures (a) Mosfet biased at ZTC Point (b)

As it is visible in the image above us, working with 0.250 μm technology and with appropriate sizing of a MOSFET it's possible to find the correct bias point. In this instance (a), with the mosfet sized to $W=300\text{nm}$ $L=250\text{nm}$ the ZTC bias point is found at approximately 0.8 V.

Looking at figure (b) that shows the same mosfet device now biased at the ZTC point previously determined. We can see a maximum of 328 nA of variation around a medium of 16.05 μA . This gives us an accuracy of around 2.04% from a -60°C to 140°C

This test was conducted assuming an ideal voltage source under typical conditions.

MOS Bandgap

In this section I will be presenting the results of a simple simulation of a conventional bandgap voltage reference. The circuit itself is rather simple and provides only temperature compensation. It has the standard Wilson mirror on the top with a single resistor in one of the branches.

Connected to these mirror are two diode connected PMOS that were originally vertical BJT. The lack of BJT model makes it impossible to show the results of a traditional bandgap [1] or even its improved, low voltage model [11].

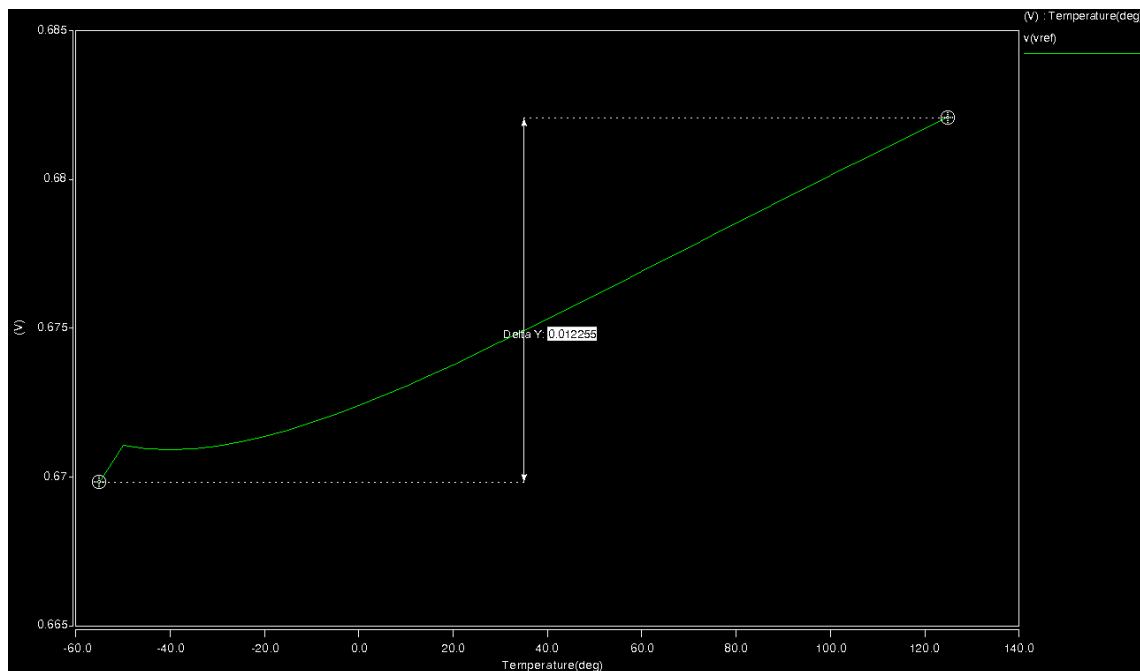


Figure 4.2 Current shift under Temperature

Analyzing the figure above, we can clearly see that using the standard bandgap techniques gives us a fairly accurate voltage. This simulation used 45nm technology and gives an accuracy of 1.22% within a 200°C margin.

Please note that this simulation has no supply or process compensation.

This test was conducted assuming an ideal voltage source under typical conditions.

Chapter 5

Work Plan

A work plan for this thesis has been already proposed and it contains the more important milestones for this work. The delivery of this report marks the completion of the first step, which is literature review and state-of-the-art.

The next step would be in-depth study of the more relevant topologies. It will be fundamental a thorough understanding of how the circuits behave, specifically their strengths and shortcomings in the context of this thesis main goals. During this phase, the more relevant architectures will be simulated using *Mathworks MATLAB and Synopsis HSPICE*. The objective at the end of this step is to have a well-defined system architecture that meets our goals and performs adequately at both system and circuit level.

Once the planning phase has been concluded we will proceed with the implementation phase. During this stage all efforts will be directed towards implementing the defined circuit in a specific process, which implies a more careful device selection, tuning of component values, and extensive transistor-level simulations like monte-carlo and full corners.

The next step after the simulations would be a more “physical” implementation of the circuit. Once the circuit has passed all the required conditions the next step would be creating the layout using a *Layout Suite*, followed by a full post-layout validations using *Synopsys HSPICE*. The objective of this phase is to realize the previous simulated circuit into a state as close to production-ready as possible.

Lastly, the final step would be writing the final report. Efforts will be made to parallelize our work with the writing of the final report, in a *write-as-you-go* style. A table depicting the work plan and deadlines is presented below.

Milestone	Deadline
Literature Review	18-02-2015
Final Architecture	31-03-2015
Layout Implementation	20-04-2015
Delivery Final Report	30-06-2015

Table 5.1 Work Plan

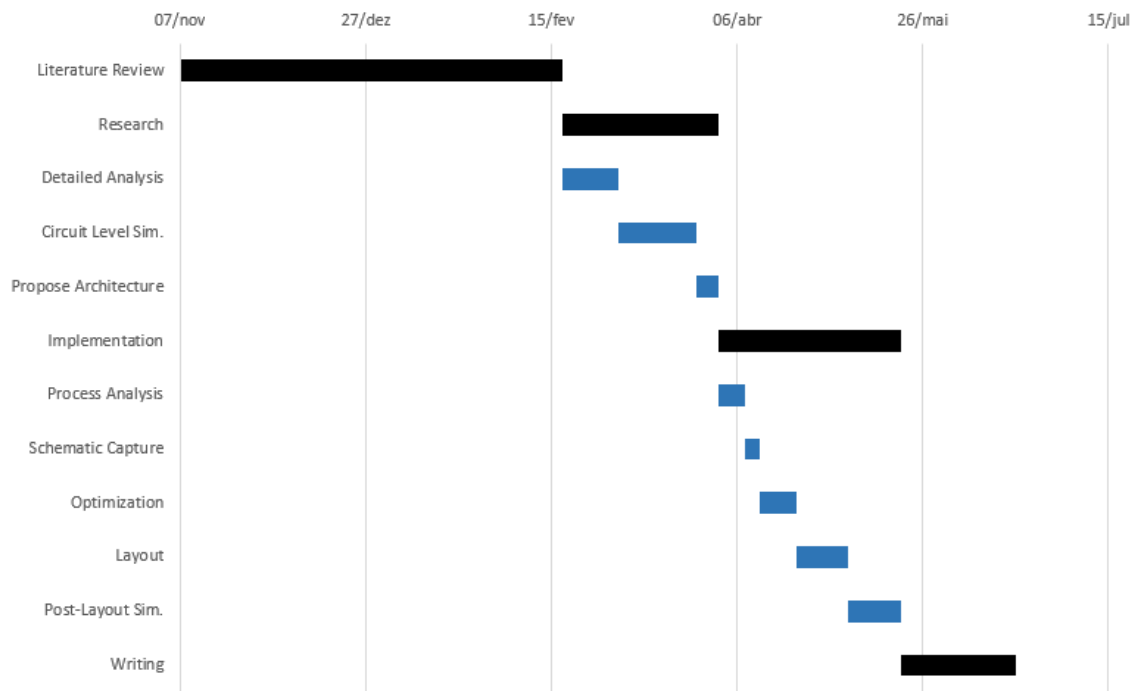


Figure 5.1 – Gantt chart for thesis work plan

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